QP CODE: 23800329

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Reg No : .....

Name : .....

INTEGRATED PG DEGREE EXAMINATION, DECEMBER 2023

Third Semester

INTEGRATED MSC COMPUTER SCIENCE-ARTIFICIAL INTELLIGENCE AND MACHINE LEARNING

Complementary - ICSA3CM5 - DIGITAL ELECTRONICS

2020 ADMISSION ONWARDS

DFAC487A

Time: 3 Hours | Weightage: 30

Part A (Short Answer Questions)

*Answer any **eight** questions.*

*Weight **1** each.*

1. Define Binary Addition and Binary substraction.
2. Add the following hexadecimal numbers
   a) $(4C)_{16} + (3A)_{16}$
   b) $(18)_{16} + (34)_{16}$
3. Draw the truth table of XNOR gate for two variables.
4. Design XNOR gate using NOR gates.
5. Apply De-Morgan's theorems to each expression
   a) ((A+B)'+C')'
   b) ((A'+B)+CD)'
6. Find the standard Product of Sum (POS) for the logic expression F=(A + B'C) C
7. What is data distributor.
8. Define Race Around Condition.
9. How many flip-flops are required to build a binary counter that counts from 0 to 1023?
10. Define mod number.

(8×1=8 weightage)

Part B (Short Essay/Problems)

*Answer any **six** questions.*

*Weight **2** each.*

11. (i) Convert $(725.25)_{10}$ to its Binary and Hexadecimal equivalent.
    (ii) Find 1's and 2's Complement of 8 digit binary number 10101101.
12. Draw the logic circuits for the realization of AND, OR and NOT operations using NAND gates only and using NOR gates only.
13. Explain about Boolean postulates and laws.
14. Convert the following boolen expression into its Canonical POS form:
    a) F = (B + C') .(A' + B)
    b) Y= (A + B). (A' + C). (A' + B + C) .(B' + C)
15. Explain about 2-bit Magnitude Comparator.
16. Draw the logic diagram of J-K flip flop and explain it. What is the advantage of J-K flip flop over S-R flip flop.
17. Explain briefly about Serial in- Parallel out shift registers with neat sketch.
18. Describe shift registers and explain 4-bit bidirectional shift register with parallel load.

(6×2=12 weightage)

Part C (Essay Type Questions)

*Answer any **two** questions.*

*Weight **5** each.*

19. Simplify using K-map to obtain minimum POS expression (A'+B'+C+D) (A+B'+C+D) (A+B+C+D') (A+B+C'+D') (A'+B+C+D') (A+B+C'+D).
20. Explain the Implementation of Full Adder using Half Adders.
21. What is Latches? Write about the operations of different latches.
22. Design and discuss steps of asynchronous sequential circuit.

(2×5=10 weightage)