QP CODE: 24800757

24800757

Reg No : .....

Name : .....

IMCA DEGREE EXAMINATION , FEBRUARY 2024

Second Semester

Faculty of Technology & Applied Science

Integrated MCA

CORE - IMCA2C03 - COMPUTER ORGANIZATION AND ARCHITECTURE

2020 Admission Onwards

C0C5C4B1

Time: 3 Hours Maximum: 75 Marks

Part A

*Answer any **ten** questions*

*Each question carries **3** marks*

1. What do you mean by Register transfer notation?
2. Define Indexed addressing.
3. Write a note on basic input/output operations.
4. Explain execution of a complete instruction.
5. What is the usage of control step counter in the hardwired control?
6. Define microinstructions.
7. What is the role of I/O processor?
8. Write a note on primary memory.
9. Define interrupt latency and how can it be reduced.
10. Explain the process of distributed arbitration.
11. Define data dependency with example.
12. Define instruction hazard.

(10×3=30 marks)

Part B

*Answer **all** questions*

*Each question carries **9** marks*

13. a) Explain the memory locations and addresses organized in the memory.

OR

b) Briefly describe the instruction sequencing.

14. a) Explain the hardwired control in detail.

OR

b) Explain microprogrammed control unit with neat diagram.

15. a) What is main memory?What are the functions of main memory?Explain in detail.

OR

b) Explain in detail the concepts of virtual memory.

16. a) Discuss the method of handling multiple interruts.

OR

b) Explain the function of DMA controller with suitable diagram.

17. a) Explain the methods to improve pipline performance

OR

b) Explain instruction pipline in detail.

(5×9=45 marks)